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(54) DATA PROCESSING METHOD FOR GENERATING ERROR CORRECTION PRODUCT CODE BLOCK, DATA PROCESSING METHOD FOR RECORDING DATA IN RECORDING MEDIUM, AND DATA PROCESSING DEVICE FOR DATA

(57) There is provided a method of processing data for generating an error correcting product code block devised so as to maintain the current level of redundancy after the error correcting ability is modified as a result of advancement of the technologies of semiconductor and data recording/transmission. Unlike any known technique of configuring a Reed-Solomon error correcting product code block of (M+P0)×(N+PI) bytes for an information data of (M×N) bytes, an error correcting product code block data structure is obtained by configuring a (K×(M+1)×(N+P))-byte Reed-Solomon error correcting product code block for a (K×M×N)-byte data and making K variable to consequently make the entire size of the Reed-Solomon error correcting product code block variable and, at the same time, the error correcting ability variable in proportion to the value of K without increasing the redundancy.

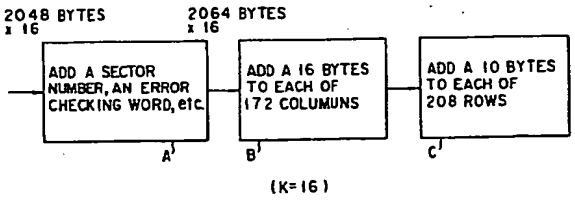

FIG. 2

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Description

Technical Field

This invention relates to a method of configuring an error correcting product code block adapted for use for digital data recording/transmission and, more particularly, it relates to a method of processing data for generating an error correcting product code block devised so as not to change the level of redundancy after the error correcting ability is modified. The present invention also relates to a method of processing data for recording such data on a recording medium as well as to an apparatus for processing such data.

Background Art

In a system for recording digital data by using the unit of byte, which is equal to eight bits, data are processed by configuring Reed-Solomon error correcting product code blocks. More specifically, after arranging data of (M×N) bytes in M rows × N columns, a P0-byte error correcting check word is added to the N-byte information section of each column and then a PI-byte error correcting check word is added to the N-byte information section of each row to produce a Reed-Solomon error correcting product code block comprising (M+P0) rows × (N+PI) columns. Then, random errors and burst errors can be efficiently corrected on the data reproducing side or the data receiving side by means of the Reed-Solomon error correcting product code blocks that is recorded and transmitted.

A Reed-Solomon error correcting product code block as described above operates efficiently when the redundancy is large or the ratio of the redundant section of the error correcting check word (PI×M+P0×N+PI×P0) to the entire code word (M+P0)×(N+PI) is small. On the other hand, its error correcting ability is raised for both random errors and burst errors when large values are used for PI and P0.

It is known that, when different Reed-Solomon error correcting product code blocks having a same level of redundancy are compared, those having small M, N, PI and P0 are poorly adapted for error correcting because the probability of occurrence of error correction rises with such code blocks.

On the other hand, while it is also known that the error correcting ability of a Reed-Solomon error correcting product code block is raised by increasing the values of M and N because the values of PI and P0 are also increased accordingly, if the redundancy is held to a same level, such high error correcting ability cannot be realized without satisfying the requirements as will be described below.

Firstly, in terms of code word length that allows a Reed-Solomon code word to be configured, M+P0 and N+PI have to be equal to or less than 255 bytes.

Secondly, there is a hardware cost restriction to be observed. Specifically, it is expressed typically in terms of the cost of the operational circuit and that of the memory for storing the entire code word or (M+P0)×(N+PI) bytes. Since the cost of a memory can change with the development of semiconductor technology, it is highly desirable to make the above described parameters of M, N, PI and P0 of Reed-Solomon error correcting product code block variable as a function of the advancement of semiconductor technology and, particularly, the reduction in the cost of a memory.

This is because a same error in a physical length or a time length is translated into a larger burst error bytes as the density with which data are recorded on a medium or the rate at which data are transmitted through a transmission path is raised in accordance with the advancement of semiconductor technology so that a higher error correcting ability becomes necessary.

Conventionally, however, a Reed-Solomon error correcting product code block having (M+P0)×(N+PI) bytes is configured for a given data of (M×N) bytes so that the redundancy is automatically set as a function of the entire size of the product code block. In other words, any attempt for maintaining a given level of error correcting ability is accompanied by a problem of invariable block size.

However, as a higher recording density and a higher transmission rate are expected with the advancement of semiconductor technology in the future, a much more higher level of error correcting ability will be required for an error correcting product code block of a given size. This in turn requires the use of a large error correcting check word, although it entails an enhanced level of redundancy if the conventional technology is used.

Disclosure of the Invention

It is, therefore, an object of the present to provide a method of processing data for generating an error correcting product code block devised so as to maintain the current level of redundancy after the error correcting ability is improved as a result of advancement of the technologies of semiconductor and data recording/transmission. It is another object of the present invention to provide a method of processing data for recording such data on a recording medium as well as to an apparatus for processing such data.

According to the invention, the above objects are achieved by providing an error correcting product code block data structure obtained by configuring a (K×(M+1)×(N+P))-byte Reed-Solomon error correcting product code block for a

(K×M×N)-byte data and making K variable to consequently make the entire size of the Reed-Solomon error correcting product code block variable and, at the same time, the error correcting ability variable in proportion to the value of K.

More specifically, there is provided a method of generating an error correcting product code block comprising:

a first step of processing digital data on a byte by byte basis to configure an information data block out of bytes of N rows × N columns (M×N bytes), arranging data on a byte by byte basis in the information data block and arranging data in each row sequentially from the 0th to the (N-1)-th column according to the sequence of data transmission and sequentially from the 0th to the (M-1)-th row according to the sequence of data transmission;

a second step of arranging a matrix block of (K×M) rows × N columns by using K information data blocks arranged sequentially according to the sequence of data transmission;

a third step of adding an error correcting check word of K bytes to each column of (K×M) bytes of the matrix block to turn each of N rows into a Reed-Solomon code word C2 of (K×(M+1)) bytes; and

a fourth step of adding an error correcting check word of P bytes to each row of N bytes to turn each of the (K×(M+1)) rows into a Reed-Solomon code word C1 of (N+P) bytes;

the error correcting product code block being a Reed-Solomon error correcting product code block of (K×(M+1)×(N+P)) bytes having an information section of K information data blocks of (K×M×N) bytes, the sum of (M×N) bytes of an information data block and the average number of bytes of a check word added thereto being held to a constant value of (M+1)×(N+P) bytes.

With the above method, the sum of (M×N) bytes of an information data block and the average number of bytes of a check word added thereto is held to a constant value of (M+1)×(N+P) that is not dependent on the number of information data blocks, or K, of the error correcting product code block and hence the level of redundancy of the (M+1)×(N+P) bytes is maintained invariable.

According to the invention, there are also provided a method of processing data for recording such an error correcting product code block, a recording medium for recording such an error correcting product code block and a telecommunication apparatus for transmitting such an error correcting product code block.

Brief Description of the Drawings

FIG. 1 is an illustration showing the configuration of a known Reed-Solomon error correcting product code block;

FIG. 2 is a block diagram showing the procedure of generating a Reed-Solomon error correcting product code block according to an embodiment of the invention;

FIG. 3 is an illustration showing the configuration of a Reed-Solomon error correcting product code block generated by the procedure of FIG. 2;

FIG. 4 is an illustration showing the configuration of sectors of a Reed-Solomon error correcting product code block generated by a method according to the invention;

FIG. 5 is a block diagram showing the procedure of generating a Reed-Solomon error correcting product code block according to another embodiment of the invention;

FIG. 6 is an illustration showing the configuration of a Reed-Solomon error correcting product code block generated by the procedure of FIG. 5;

FIG. 7 is a block diagram showing the procedure of generating a Reed-Solomon error correcting product code block according to still another embodiment of the invention; and

FIG. 8 is an illustration showing the configuration of a Reed-Solomon error correcting product code block generated by the procedure of FIG. 7.

Best Mode for Carrying Out the Invention

Now, the present invention will be described by referring to the accompanying drawings that illustrate preferred embodiments of the invention.

FIG. 1 is an illustration showing the configuration of a known Reed-Solomon error correcting product code block. With this known format, as described earlier, a Reed-Solomon error correcting product code block of (M+P0)×(N+PI) bytes is configured for an information data of (M×N) bytes and, therefore, the level of redundancy and the size of the entire block is closely tied to each other so that the size of the block cannot be arbitrarily changed without modifying the error correcting ability. In other words, the level of redundancy is inevitably and undesirably raised if a large error correcting check word is used.

Contrary to this, according to the invention, a Reed-Solomon error correcting product code block is configured in a manner as illustrated in FIG. 2.

In a first embodiment, which will be described hereinafter, values of K=16, M=12, N=172 and P=10 are selected for recording a data of 2,048 bytes in a sector of a recording medium, which may preferably be an optical disc.

In this embodiment, P=10 bytes is selected for code word C1 and K=16 bytes is selected for cord word C2 as the number of bytes of error correcting check word in view of the fact that an even number is more efficient than an odd number for a same error correcting ability, that a required level of burst error correcting ability cannot be maintained for K=16 rows if P=8 bytes or less because of a rise in the probability of error correction and that a relationship of K>P is required to raise the level of burst error correcting ability for a same level of redundancy. Additionally, values of M=12 and N=172 are selected in view of the fact that the size of a sector has to be slightly larger than 2,048 bytes because a sector number and an error detecting word have to be added to a recorded data of 2,048 bytes for each sector.

FIG. 2 is a block diagram showing the procedure of generating a Reed-Solomon error correcting product code block by using a unit of 16 sectors. FIG. 3 is an illustration showing the row configuration of a Reed-Solomon error correcting product code block in a sector.

Referring to block A through C of FIG. 2, in the first step, a digital data is processed on a byte by byte basis to form an information data block with (M×N) bytes of M (=12) rows × N (=172) columns and data are arranged on a byte by byte basis in the information data block, while data are arranged sequentially in each row from the 0th to the (N-1)-th column according to the sequence of data transmission and sequentially from the 0th to the (M-1)-th row according to the sequence of data transmission.

Then, in the second step, a matrix block of (K×M) rows × N columns is arranged by using K (=16) information data blocks, each having a configuration as described above.

Subsequently, in the third step, an error correcting check word of K (=16) bytes is added to each column of (K×M) bytes of the matrix block to turn each of N rows into a Reed-Solomon code word C2 of (K×(M+1)) bytes.

Finally, in the fourth step, an error correcting check word of P (=10) bytes is added to each row of N bytes to turn each of the (K×(M+1)) rows into a Reed-Solomon code word C1 of (N+P) bytes.

The entire error correcting product code block is a Reed-Solomon error correcting product code block of (K×(M+1)×(N+P)) bytes having an information section of K information data blocks of (K×M×N) bytes. The sum of (M×N) bytes of an information data block and the average number of bytes of a check word added thereto is held to a constant value of (M+1)×(N+P) bytes.

This embodiment will be described further by referring to FIGS. 2, 3 and 4.

A data to be recorded is taken in by 2,048 bytes at a time for a sector, to which a sector number and an error detecting word (16 bytes) are added for the sector to make the total number of bytes equal to 2,064. (See block A of FIG. 2.) As shown in FIG. 4, a total of 16 bytes are used for a sector number (ID; sector identification), an ID error correcting word (IEC), a system reservation code (RSV) and an error detecting code (EDC).

The 2,064 bytes are assigned to a sector of a Reed-Solomon error correcting product code block and stored in the storage area of M rows × N columns = 12 rows × 172 columns = 2,064 bytes obtained by subtracting the storage area for an error correcting check word from the overall storage area of a sector of (M+1) rows × (N+P) columns = 13 rows × 182 columns .

In this way, the data is sequentially stored into K=16 sectors of memory.

After storing a data of 192 rows × 172 columns in K=16 sectors, each of the 172 columns are processed to produce a Reed-Solomon code word C2 of (192+16) bytes to fill the 16 void rows, each of which is arranged for every 20 rows (as indicated by X in FIG. 3). (See block B of FIG. 2.)

The relationship between the 16 rows to be filled with Reed-Solomon code words and the degree of the Reed-Solomon code word C2 is determined in advance such that the positions of the 16 rows and the degree show a one-to-one correspondence or the former correspond to a lower degree side of the 15th down to the 0th.

After filling the 16 void rows (X), an error correcting check word of 10 bytes is added to each row of the matrix of 208 rows × 172 columns to form a (172+10)-byte Reed-Solomon code word C1 for each of the 208 columns. Thus, a Reed-Solomon error correcting product code block is formed as shown in FIG. 3 by using a unit of 16 sectors. (See block C of FIG. 2.)

The block has a size of 208 rows × 182 columns = 37,856 bytes that can be optimally stored with a generous margin in a memory device that is currently commercially available at low cost.

The redundancy of a Reed-Solomon error correcting product code block realized by using a unit of 16 sectors is equal to

$$(208 \times 182 - 192 \times 172) / (208 \times 182) = 12.76\%$$

while a correctable burst error has a maximum length that can be obtained on the basis of the number of rows corresponding to the number of error correcting check words C2, or 16 rows × 182 columns = 2,912 bytes.

As a correctable burst error has a maximum length that can be obtained on the basis of the number of rows corresponding to the number of error correcting check words C2, the error correcting ability can be improved by increasing the number of rows and that of error correcting check words C2 of a Reed-Solomon error correcting product code block.

Thus, the level of redundancy can be maintained to a constant level with the above described method of the present invention because the information data is always allocated to the sectors in a manner as illustrated in FIG. 4.

Situations where the number of rows and that of error correcting check words have to be increased for a Reed-Solomon error correcting product code block may include those where the error correcting ability has to be raised and those where the recording density per given length of the tracks of an optical disc as a result of advancement of the technologies of semi-conductor and data recording/transmission. If such is the case, the number of error correcting check words C2 can be increased by increasing the number of rows of the block. For reproducing the stored information, the stored pieces of information are sequentially picked up along the rows of the block and, with the above described method of the present invention, a same level of redundancy can be maintained if the stored Reed-Solomon error correcting product code block is taken up for error correction.

While a figure of K=16 is used in the above description, it may be needless to say that K=12 may be selected depending on the memory size. Then, a less costly memory device may be used for the purpose of the invention since the size of block is 28,392 byte which can be stored in 256 Kbit capacity.

FIG. 5 is a block diagram showing the procedure of generating a Reed-Solomon error correcting product code block according to a second embodiment of the invention. Note that K=12 in this embodiment. Blocks 5A, 5B and 5C of FIG. 5 correspond to blocks A, B and C in FIG. 2 respectively.

FIG. 6 is an illustration showing the configuration of a Reed-Solomon error correcting product code block generated by the procedure of FIG. 5.

FIG. 7 is a block diagram showing the procedure of generating a Reed-Solomon error correcting product code block according to a third embodiment of the invention. FIG. 8 is an illustration showing the configuration of a Reed-Solomon error correcting product code block generated by the procedure of FIG. 7.

As shown, a data to be recorded is taken in by 2,048 bytes at a time for a sector, to which a sector number and an error detecting word (16 bytes) are added for the sector to make the total number of bytes equal to 2,064. (See block 7A of FIG. 7.) The 2,064 bytes are assigned to a sector of a Reed-Solomon error correcting product code block and stored in the storage area of M rows × N columns = 12 rows × 172 columns = 2,064 bytes obtained by subtracting the storage area for an error correcting check word from the overall storage area of a sector of (M+1) rows × (N+P) columns = 13 rows × 182 columns .

In this way, the data is sequentially stored into K=18 sectors of memory.

After storing a data of 216 rows × 172 columns in K=18 sectors, each of the 172 columns are processed to produce a Reed-Solomon code word C2 of (216+18) bytes to fill the 18 void rows, each of which is arranged for every 12 rows (as indicated by X in FIG. 8). (See block 7B of FIG. 7.)

After filling the 18 void rows (X), an error correcting check word of 10 bytes is added to each row of the matrix of 234 rows × 172 columns to form a (172+10)-byte Reed-Solomon code word C1 for each of the 234 columns. Thus, a Reed-Solomon error correcting product code block is formed as shown in FIG. 8 by using a unit of 18 sectors. (See block 7C of FIG. 7.)

This embodiment can raise the error correcting ability relative to the preceding embodiments, although the level of redundancy remains same.

As described above in detail, there is provided a method of processing data for generating an error correcting product code block devised so as to maintain the current level of redundancy after the error correcting ability is improved as a result of advancement of the technologies of semiconductor and data recording/transmission.

Industrial Applicability

This invention is useful to recording and transmitting of digital data, and is effectively used to a recording/reproducing system, a transmitting/receiving system and a data processing system for an optical disc.

Claims

1. A method of processing data by generating an error correcting product code block comprises:

   a first step of processing digital data on a byte by byte basis to configure an information data block out of (M×N) bytes of N rows × N columns, arranging data on a byte by byte basis in said information data block and arranging data in each row sequentially from the 0th to the (N-1)-th column according to the sequence of data transmission and sequentially from the 0th to the (M-1)-th row according to the sequence of data transmission;
   a second step of arranging a matrix block of (K×M) rows × N columns by using K information data blocks arranged sequentially according to the sequence of data transmission;
   a third step of adding an error correcting check word of K bytes to each column of (K×M) bytes of the matrix block to turn each of N rows into a Reed-Solomon code word C2 of (K×(M+1)) bytes; and
   a fourth step of adding an error correcting check word of P bytes to each row of N bytes to turn each of the (K×(M+1)) rows into a Reed-Solomon code word C1 of (N+P) bytes;
   said error correcting product code block being a Reed-Solomon error correcting product code block of

(K×(M+1)×(N+P)) bytes having an information section of K information data blocks of (K×M×N) bytes, the sum of (M×N) bytes of an information data block and the average number of bytes of a check word added thereto being held to a constant value of (M+1)×(N+P) bytes.

2. A method of processing data to record the data in a recording medium by generating an error correcting product code block comprises:

a first step of processing digital data on a byte by byte basis to configure an information data block out of (M×N) bytes of N rows × N columns, arranging data on a byte by byte basis in said information data block and arranging data in each row sequentially from the 0th to the (N-1)-th column according to the sequence of data transmission and sequentially from the 0th to the (M-10)-th row according to the sequence of data transmission;
a second step of arranging a matrix block of (K×M) rows × N columns by using K information data blocks arranged sequentially according to the sequence of data transmission;
a third step of adding an error correcting check word of K bytes to each column of (K×M) bytes of the matrix block to turn each of N rows into a Reed-Solomon code word C2 of (K×(M+1)) bytes; and
a fourth step of adding an error correcting check word of P bytes to each row of N bytes to turn each of the (K×(M+1)) rows into a Reed-Solomon code word C1 of (N+P) bytes;
said error correcting product code block being a Reed-Solomon error correcting product code block of (K×(M+1)×(N+P)) bytes having an information section of K information data blocks of (K×M×N) bytes, the sum of (M×N) bytes of an information data block and the average number of bytes of a check word added thereto being held to a constant value of (M+1)×(N+P) bytes.

3. A method of processing data according to any one of claims 1 and 2, wherein, in said third step, an error correcting check word of K bytes is added to the tail end of each row of (K+M) bytes to form a Reed-Solomon code word C2 of (K×(M+1)) bytes for each of the N rows and subsequently the error correcting check word of K bytes is redistributed on a byte by byte basis to a position of every M bytes of information data.

4. A method of processing data according to any one of claims 1 and 2, wherein, in said third step, said Reed-Solomon error correcting code word C2 of (K×(M+1)) bytes is formed by arranging a one byte position in every M bytes for each of the K bytes of the error correcting check word to be added to each row of (K×M) bytes.

5. A method of processing data according to any one of claims 1 and 2, wherein said M×N is not smaller than 2,054 and not greater than 2,064, said K is an even number not smaller than 12, said P is an even number not smaller than 10, said K×(M+1) is not greater than 255, said N+P is not greater than 255.

6. A method of processing data according to any one of claims 1 and 2, wherein M=12, N=172, K=16 and P=10.

7. A method of processing data according to any one of claims 1 and 2, wherein M=12, N=172, K=12 and P=10.

8. A method of processing data according to any one of claims 1 and 2, wherein M=12, N=172, K=18 and P=10.

9. A recording medium as defined by claim 2, wherein said error correcting product code block is recorded there.

10. A recording medium as defined by claim 2, wherein an information data block of (M×N) bytes of said error correcting product code block is correspondingly recorded in a sector.

11. A data processing apparatus comprises means for processing an error correcting product code block configured by:

processing a digital data on a byte by byte basis to configure an information data block by (M×N) bytes of M rows × N columns;
arranging data on a byte by byte basis in said information data block and arranging data in each row sequentially from the 0th to the (N-1)-th column according to the sequence of data transmission and sequentially from the 0th to the (M-10)-th row according to the sequence of data transmission;
arranging a matrix block of (K×M) rows × N columns by using K information data blocks arranged sequentially according to the sequence of data transmission;
adding an error correcting check word of K bytes to each column of (K×M) bytes of the matrix block to turn each of N rows into a Reed-Solomon code word C2 of (K×(M+1)) bytes; and
adding an error correcting check word of P bytes to each row of N bytes to turn each of the (K×(M+1)) rows

into a Reed-Solomon code word C1 of (N+P) bytes;

said error correcting product code block being a Reed-Solomon error correcting product code block of (K×(M+1)×(N+P)) bytes having an information section of K information data blocks of (K×M×N) bytes, the sum of (M×N) bytes of an information data block and the average number of bytes of a check word added thereto being held to a constant value of (M+1)×(N+P) bytes.

12. A data processing apparatus according to claim 11, wherein said means for processing an error correcting product code block is arranged in a telecommunications apparatus, a data recording apparatus for recording data onto a disc or an error correction processing apparatus.

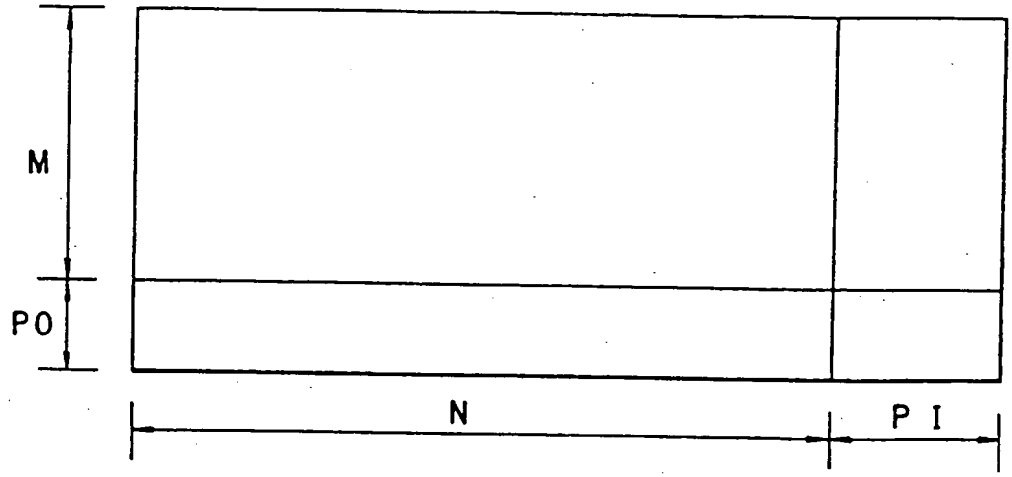
M
P0
N
P I

FIG. 1

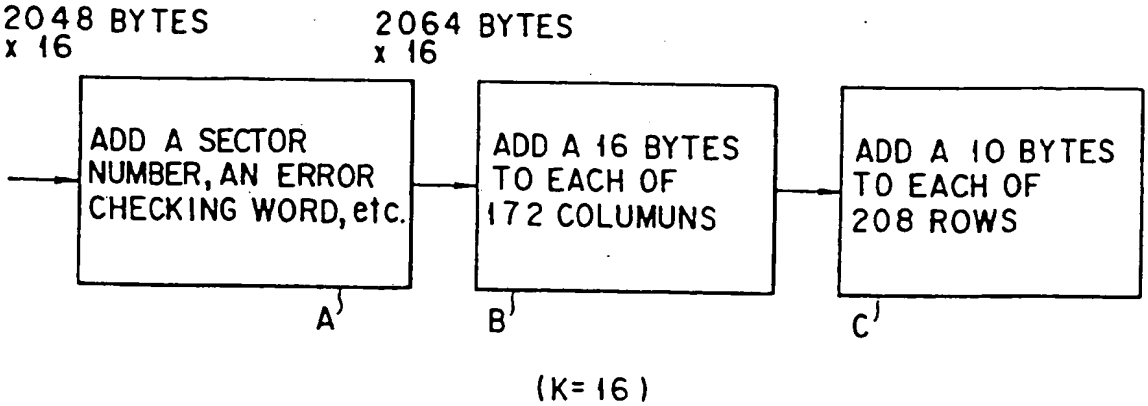
2048 BYTES
x 16
2064 BYTES
x 16
ADD A SECTOR NUMBER, AN ERROR CHECKING WORD, etc.
ADD A 16 BYTES TO EACH OF 172 COLUMUNS
ADD A 10 BYTES TO EACH OF 208 ROWS
A
B
C
(K=16)

FIG. 2

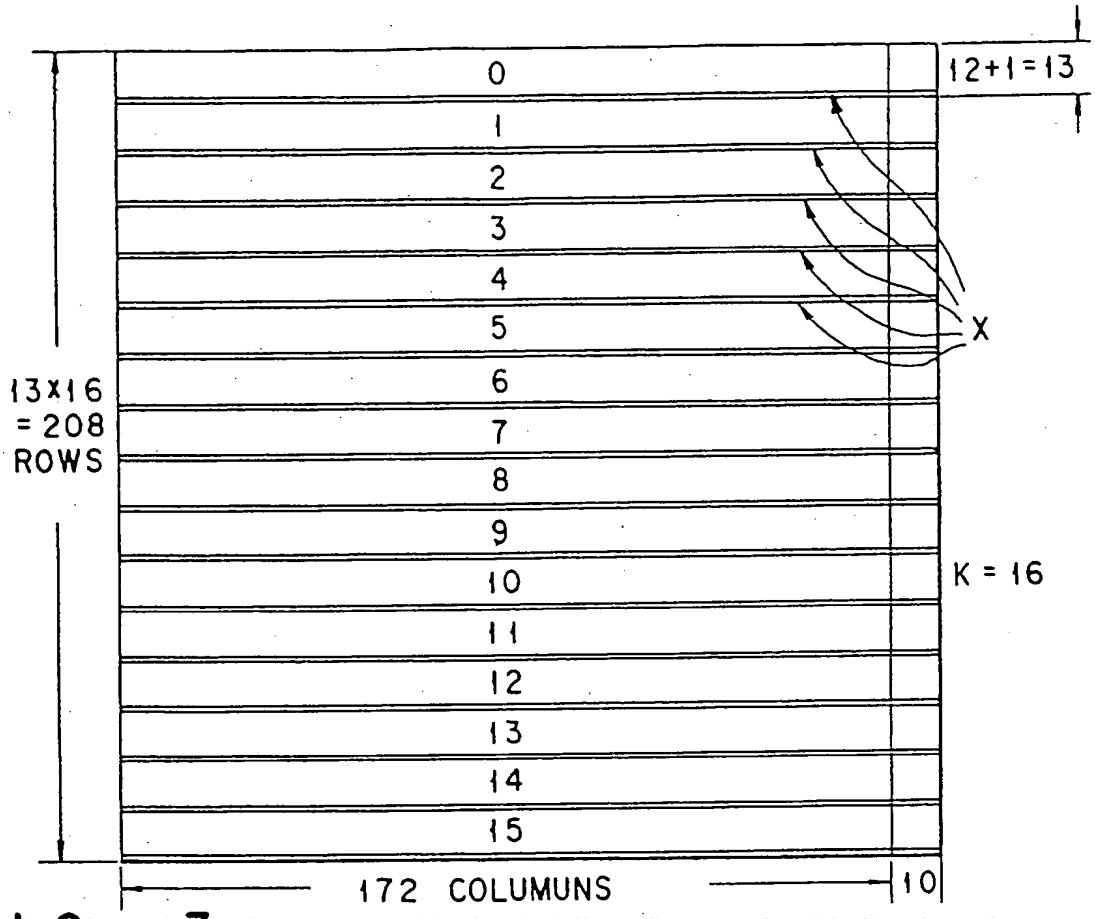
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
12+1=13
X
13x16
=208
ROWS
K = 16
172 COLUMUNS
10

FIG. 3

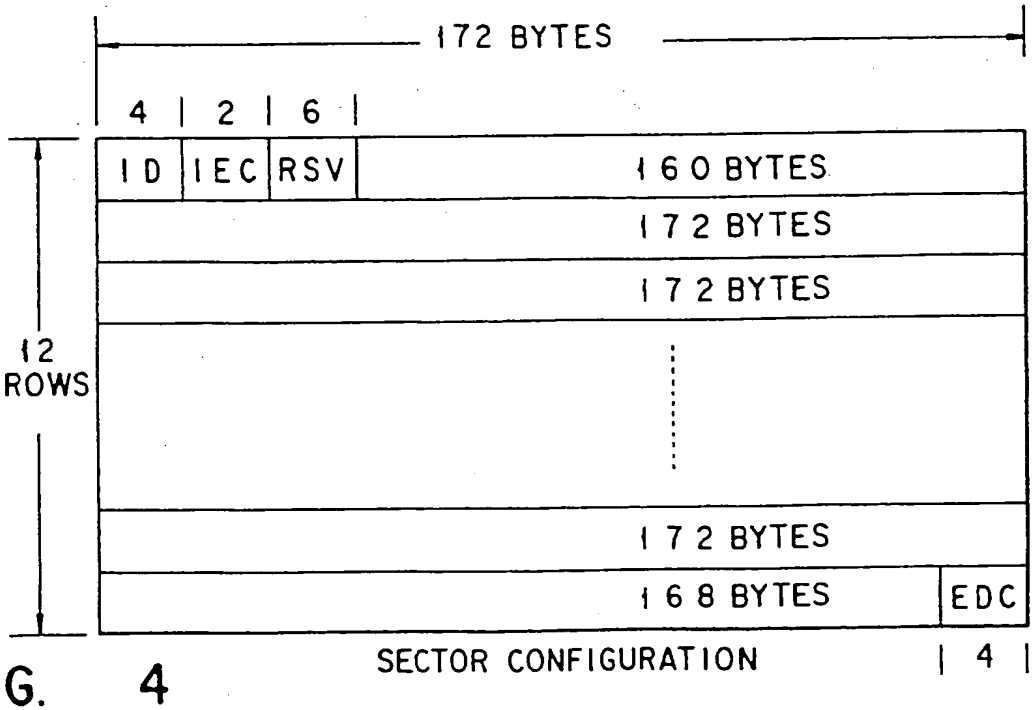
172 BYTES
4
2
6
ID
IEC
RSV
160 BYTES
172 BYTES
172 BYTES
12
ROWS
172 BYTES
168 BYTES
EDC
SECTOR CONFIGURATION
4

FIG. 4

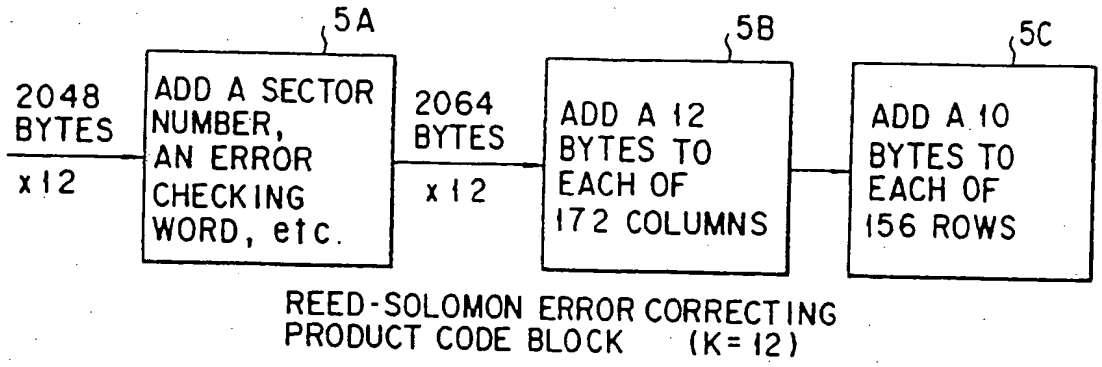
5A
5B
5C
2048 BYTES
x 12
ADD A SECTOR NUMBER, AN ERROR CHECKING WORD, etc.
2064 BYTES
x 12
ADD A 12 BYTES TO EACH OF 172 COLUMNS
ADD A 10 BYTES TO EACH OF 156 ROWS
REED-SOLOMON ERROR CORRECTING PRODUCT CODE BLOCK (K=12)

FIG. 5

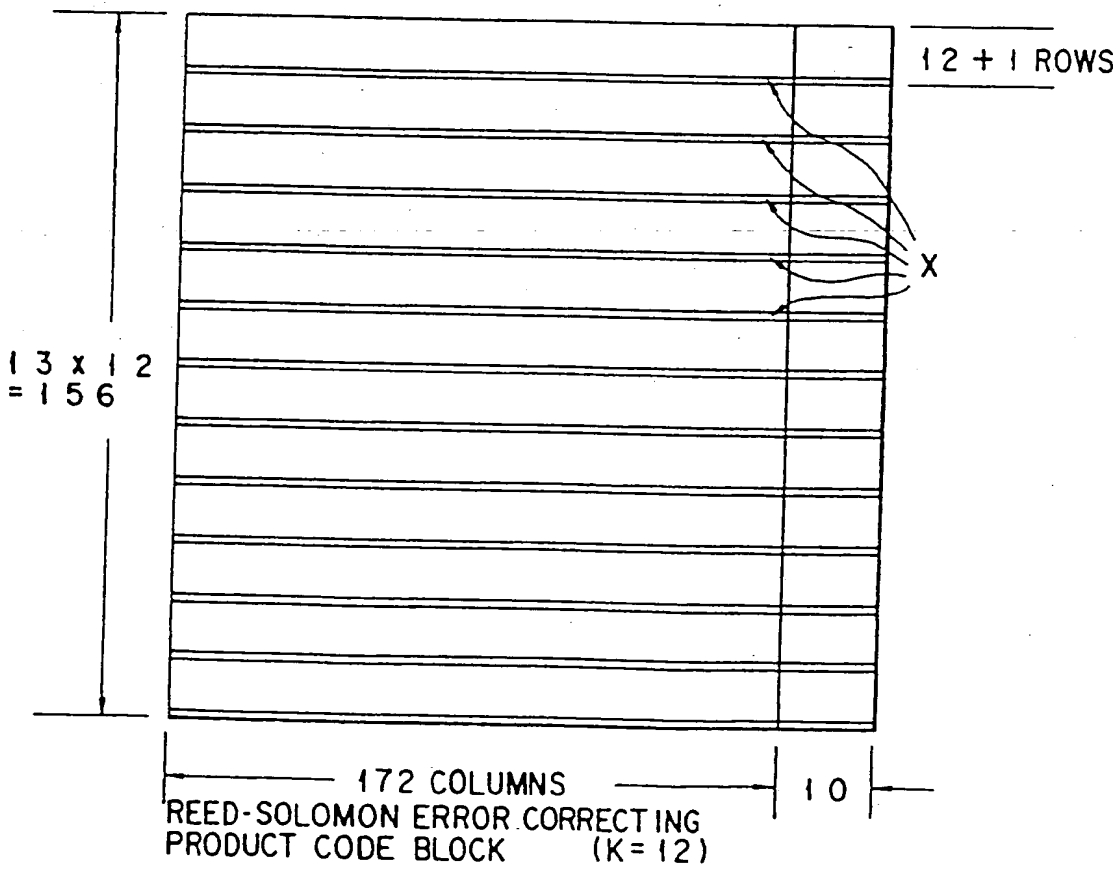
12 + 1 ROWS
X
13 x 12 = 156
172 COLUMNS
10
REED-SOLOMON ERROR CORRECTING PRODUCT CODE BLOCK (K=12)

FIG. 6

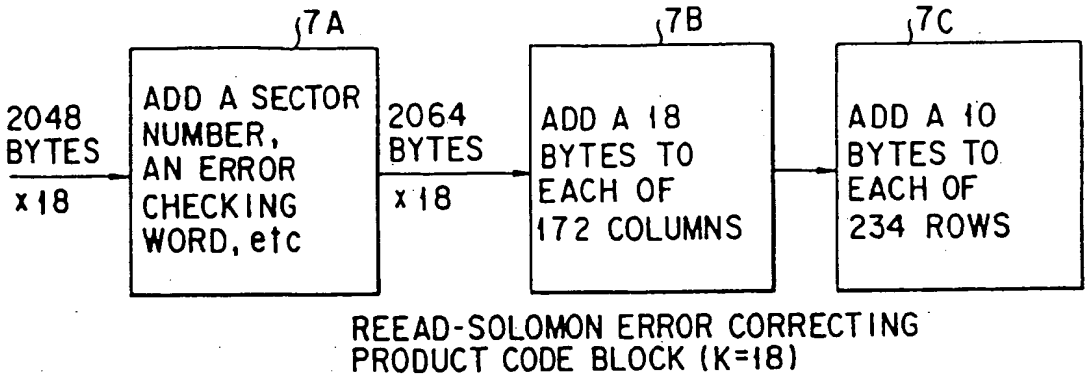
7A
7B
7C
2048 BYTES x18
ADD A SECTOR NUMBER, AN ERROR CHECKING WORD, etc
2064 BYTES x18
ADD A 18 BYTES TO EACH OF 172 COLUMNS
ADD A 10 BYTES TO EACH OF 234 ROWS
REEAD-SOLOMON ERROR CORRECTING PRODUCT CODE BLOCK (K=18)

FIG. 7

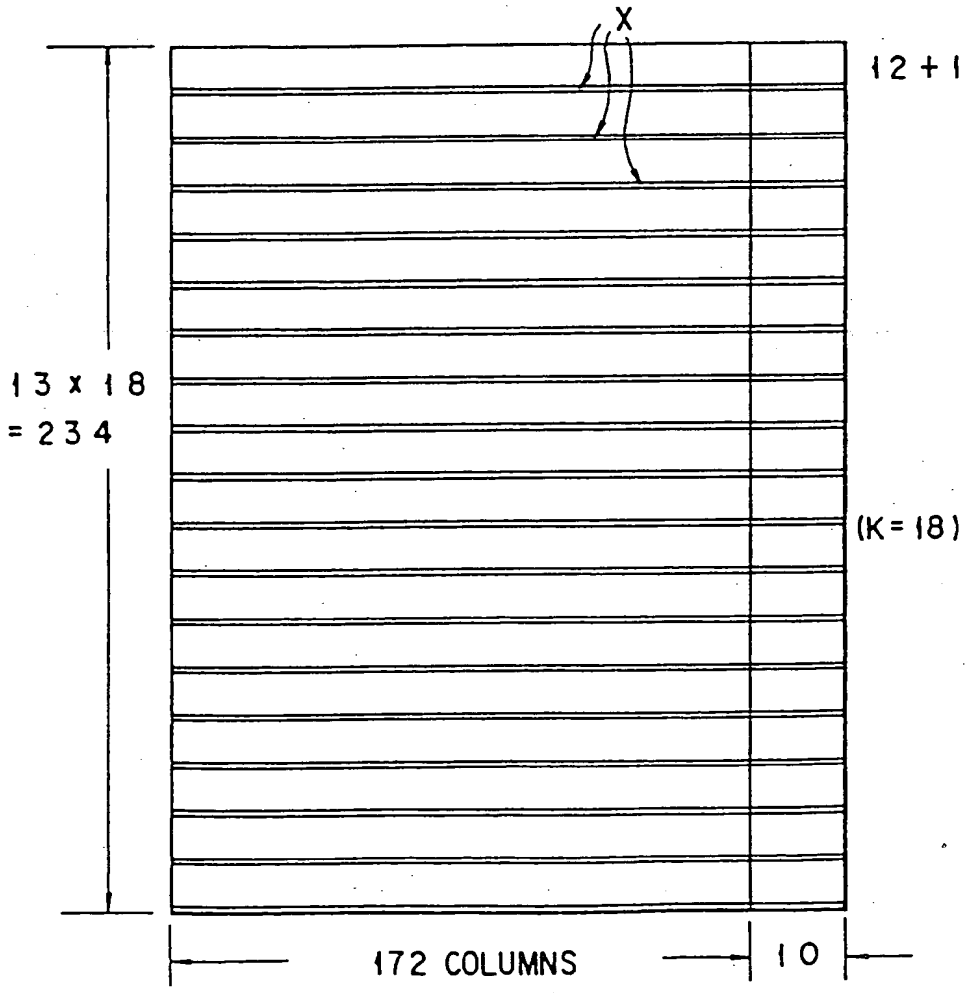
X
12 + 1
13 x 18 = 234
(K = 18)
172 COLUMNS
10
REED-SOLOMON ERROR CORRECTING PRODUCT CODE BLOCK

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP96/00956

A. CLASSIFICATION OF SUBJECT MATTER
Int. Cl^6 G11B20/12, G11B20/18, H03M13/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int. Cl^6 G11B20/12, G11B20/18, H03M13/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926 - 1996
Kokai Jitsuyo Shinan Koho 1971 - 1996
Toroku Jitsuyo Shinan Koho 1994 - 1996

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	JP, 63-23274, A (Sony Corp.), January 30, 1988 (30. 01. 88), Line 5, lower right column, page 2 to line 8, lower right column, page 3, Fig. 1 (Family: none)	1-2, 5-12 3, 4
Y	JP, 5-122197, A (Nippon Hoso Kyokai), May 18, 1993 (18. 05. 93), Lines 19 to 39, column 4, Fig. 4 & EP, 540007, A & US, 5432800, A	3, 4
A	JP, 62-171324, A (Sony Corp.), July 28, 1987 (28. 07. 87), Line 6, upper left column to line 13, lower right column, page 3 & EP, 232093, A & US, 4819236, A	1 - 12

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
May 2, 1996 (02. 05. 96)	May 14, 1996 (14. 05. 96)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

3NSDOCID: <EP 0766245A1>